IN THE CLAIMS:

1. (Currently Amended) A fault detecting method for a semiconductor integrated circuit, comprising:

providing a fault list corresponding to at least one of (a) information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, and ~~or~~ (b) information required to reduce faults; and

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detecting faults in a semiconductor integrated circuit to which said fault list corresponds, said detecting in accordance with ~~by using~~ said fault list.

2. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 1, additionally comprising:

omitting possible faults ~~that are difficult to detect~~ having a specified low probability of occurrence from the fault list to define a remaining part of the fault list, and

detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

3. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 1, wherein the fault list comprises data about a likelihood of a fault occurring at a physical site.

4. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 3, additionally comprising:

~~ordering~~ arranging the possible faults in the fault list in order according to their likelihood of occurrence to create an ordered fault list, and

detecting faults in said semiconductor integrated circuit by using the ordered fault list.

5. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 3, additionally comprising weighting possible faults at physical sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults, said fault

coverage being a probability of detecting faults in ~~said~~ a semiconductor integrated circuit, and detecting faults using a fault list comprising said weighted possible faults.

6. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 5, additionally comprising ~~ordering~~ arranging said possible faults in an order before weighting said possible faults.

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7. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 4, additionally comprising obtaining mask information from a layout device for laying out ~~the~~ a semiconductor integrated circuit to which the fault list corresponds, wherein

said ~~ordering~~ order of possible faults is based on the mask information.

8. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 4, further comprising:

calculating a density of a mask pattern corresponding to mask information obtained from a layout device for laying out the semiconductor integrated circuit to which said fault list corresponds;

calculating a likelihood of occurrence ~~of~~ for each possible ~~faults~~ fault depending on the density of the mask pattern; and

~~ordering or~~ weighting the arranged possible faults according to ~~their~~ said calculated likelihoods of occurrence.

9. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 4, additionally comprising:

providing a database storing therein reliability data based on records of past use of cells or functional blocks of ~~the~~ a semiconductor integrated circuit to which the fault list corresponds; ~~and~~ wherein

~~ordering the possible faults according to their~~ said likelihoods of occurrence~~, using~~ are according to said reliability data in the database.

10. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 6, additionally comprising:

defining a required fault list by deleting from the fault list possible faults that are not required to achieve a specified fault coverage, in an order of unlikelihood of such possible faults, said specific fault coverage being a probability of detecting faults in ~~the~~ a semiconductor integrated circuit to which said fault list corresponds; and

detecting, ~~using~~ according to said required fault list, remaining faults in ~~said~~ such semiconductor integrated circuit; and

calculating a fault coverage simultaneously with said detecting.

11. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 6, additionally comprising:

calculating ~~the~~ fault coverage simultaneously with detecting possible faults in ~~said~~ such semiconductor integrated circuit; and

terminating calculating and detecting when a specific fault coverage has been reached, said specific fault coverage being a probability of detecting faults in ~~said~~ such semiconductor integrated circuit.

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12. (Currently Amended) A fault detecting method for a semiconductor integrated circuit, comprising:

first detecting faults in a semiconductor integrated circuit to create a detection result;

combining said detection result with at least one of (a) information about physical sites ~~in~~ on a physical layout of the semiconductor integrated circuit to which said fault list corresponds where a possible fault is likely to occur ~~or~~ and (b)

information required to reduce faults, to create a fault list; and

~~using said fault list for second~~ again detecting faults according to said fault list in ~~said~~ such semiconductor integrated circuit.

13. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 12, additionally comprising:

omitting from the fault list possible faults ~~that are difficult to detect~~ having a specified low probability of occurrence to define a remaining part of the fault list, wherein

said ~~second~~ again detecting faults ~~in a semiconductor integrated circuit to which said fault list~~ comprises detecting faults according to ~~using~~ the remaining part ~~to detect faults~~ of the fault list.

14. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 12, wherein the fault list comprises data about a likelihood of a possible fault occurring at a physical site.

15. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 14, additionally comprising:

~~ordering~~ arranging the possible faults in order according to their likelihood of occurrence to create an ordered fault list, and

second detecting possible faults in ~~said~~ a semiconductor integrated circuit using the ordered fault list.

16. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 14, additionally comprising weighting possible faults at physical sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults, said fault

coverage being a probability of detecting faults in ~~said~~ a semiconductor integrated circuit, and

~~second~~ again detecting faults using a fault list comprising said weighted possible faults.

17. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 16, additionally comprising ~~ordering~~ arranging said possible faults in an order before weighting said possible faults.

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18. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 15, additionally comprising obtaining mask information from a layout device for laying out ~~the~~ a semiconductor integrated circuit to which the fault list corresponds, wherein

said ~~ordering~~ order of possible faults is based on the mask information.

19. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 15, further comprising:

calculating a density of a mask ~~patterncorresponding~~ pattern corresponding to mask information obtained from a layout device for laying out the semiconductor integrated circuit to which said fault list corresponds;

calculating a likelihood of occurrence ~~of~~ for each possible ~~faults~~ fault depending on the density of the mask pattern; and

~~ordering or~~ weighting the arranged possible faults according to ~~their~~ said calculated likelihoods of occurrence.

20. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 15, further comprising:

providing a database and storing therein reliability data based on records of past use of cells or functional blocks of ~~the~~ a semiconductor integrated circuit to which the fault list corresponds; ~~and~~ wherein

~~ordering the possible faults according to their~~ said likelihoods of occurrence~~, using~~ are according to said reliability data in the database.

21. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 17, wherein additionally comprising:

defining a required fault list by deleting from the fault list possible faults that are not required to achieve a specified fault coverage in an order of unlikelihood of such possible faults, said specific fault coverage being a probability of detecting faults in ~~the~~ a semiconductor integrated circuit to which said fault list corresponds; and

~~second~~ again detecting ~~using~~ according to said required fault list, remaining possible faults in ~~said~~ such semiconductor integrated circuit; and

calculating a fault coverage simultaneously with said second detecting.

22. (Currently Amended) The fault detecting method for a semiconductor integrated circuit according to claim 17, additionally comprising:

calculating ~~the~~ fault coverage simultaneously with detecting possible faults in ~~said~~ such semiconductor integrated circuit; and

terminating calculating and detecting when a specific fault coverage has been reached, said specific fault coverage being a probability of detecting faults in ~~said~~ such semiconductor integrated circuit.

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23. (Withdrawn) A layout method for a semiconductor integrated circuit, characterized in that:

a fault list corresponding to information on sites of a semiconductor integrated circuit where a fault is likely to occur or information required to reduce faults is used to perform mask layout and wiring for said semiconductor integrated circuit.

24. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 23, wherein the fault list contains data on likelihood of each fault.

25. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 24, wherein the mask layout and the wiring are performed for the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

26. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 24, wherein the faults are weighted with their likelihood to determine a fault coverage for the mask layout and wiring for the semiconductor integrated circuit.

27. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 26, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

28. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 25, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

29. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 25, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

30. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 25, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

31. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 27, wherein a fault coverage that can be obtained when detecting each fault is calculated, faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

32. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 27, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.

33. (Withdrawn) A layout method for a semiconductor integrated circuit, characterized in that:

detection is performed for faults in a semiconductor integrated circuit to create a fault list indicating information on sites of a semiconductor where a fault is likely to occur or information required to reduce faults so that this fault list can be used to perform mask layout and wiring for said semiconductor integrated circuit.

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34. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 33, wherein the fault list contains data on likelihood of each fault.

35. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 34, wherein the mask layout and the wiring are performed for the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

36. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 34, wherein the faults are weighted with their likelihood to determine a fault coverage for the mask layout and wiring for the semiconductor integrated circuit.

37. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 36, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

38. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 35, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

39. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 35, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

40. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 35, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

41. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 37, wherein a fault coverage that can be obtained when detecting each fault is calculated, faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of

the faults, and detecting process is conducted for the remaining faults.

42. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 37, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.

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43. (Withdrawn) A layout method for a semiconductor integrated circuit, characterized in that:

faults that are difficult to detect are omitted from a fault list before mask layout and wiring are performed based on the remaining part of the fault list for the semiconductor integrated circuit.

44. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 43, wherein the fault list contains data on likelihood of each fault.

45. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 44, wherein the mask layout and the wiring are performed for the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault.

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46. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 44, wherein the faults are weighted with their likelihood to determine a fault coverage for the mask layout and wiring for the semiconductor integrated circuit.

47. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 46, wherein the faults are ordered with their likelihood and are weighted in accordance with this ordering.

48. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 45, wherein the faults are ordered or weighted with their likelihood based on mask information obtained from a layout device for laying out the semiconductor integrated circuit.

49. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 45, wherein a density of a mask pattern is calculated based on mask information obtained from the layout device for laying out the semiconductor integrated circuit, and the faults are ordered or weighted with their likelihood depending on the density of the mask pattern.

50. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 45, wherein the faults are ordered or weighted with their likelihood using a database for reliability based on records of past use of cells or functional blocks of the semiconductor integrated circuit.

51. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 47, wherein a fault coverage that can be obtained when detecting each fault is calculated, faults that are not required to achieve a specified fault coverage are deleted in the order of the unlikelihood of the faults, and detecting process is conducted for the remaining faults.

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52. (Withdrawn) The layout method for a semiconductor integrated circuit according to claim 47, wherein the fault coverage is calculated while carrying out a process for each fault detection in accordance with the ordering, and the process is stopped once the specified fault coverage has been reached.